Fast Simulation-Based Method for Characterization of CMOS Ring Oscillators in a 180 nm Process

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***Abstract*—CMOS ring oscillators (RO) are crucial blocks in the energy management of self-powered systems since they need to guarantee oscillation at a supply headroom of about $100 \sim 150$ mV, particularly when thermoelectric and photovoltaic harvesters are used as power supplies. Due to the traditional extensive transient simulations, the characterization of ROs usually wastes a significant amount of design time. This paper proposes a fast simulation-based method to characterize CMOS ROs. The main parameters of the RO, such as its output and input total capacitances, output resistance, and transconductance, are extracted from AC simulations of the unitary-stage CMOS inverter. In addition, in view of this parameter extraction, the dynamic behavior of the RO is estimated from analytical expressions instead of the traditional extensive transient simulations.**

***Index Terms*—CMOS ring oscillator, energy management, internet-of-things (IoT), ultra-low-power (ULP).**

I. Introduction

In recent years, ultra-low-power (ULP) and ultra-low-voltage (ULV) designs have received a great deal of attention due to the continued growth of internet of things (IoT) applications. Self-powered systems based on energy harvesting are viable candidates for enhancing the power supply of systems-on-chips (SoC) [1], [2]. In energy harvesting applications, CMOS ring oscillators are crucial blocks in the design since they require supply headroom of approximately 100∼150 mV in thermoelectric and photovoltaic harvesters. Ring oscillators (ROs) and LC-based ones are the most commonly on integrated circuits [3]–[5]. These devices are characterized by poor control over their operating frequency when subjected to variations in supply voltages. As a result, sometimes a circuit to provide this control is required, such as a voltage-controlled oscillator (VCO) [6]. In RO designs, the estimation of the oscillation frequency depends on several characteristics, such as supply voltage, transistor dimensions, the number of inverters in cascade, and temperature, among others. The required time to characterize oscillators is usually based on extensive transient simulations, wasting a lot of design time.

Some methods are commonly applied to estimate the RO operation frequency, either analytically or through transient simulations, which consume a large amount of computational resources and are impractical for some applications. One of the most traditional ways to estimate the oscillation frequency is by [7]

$$f_{osc} = \frac{1}{2NT_d} \ , \tag{1}$$

which relates it with the number of stages and the constant time T_d. The estimation of the parameter T_d is challenging, mainly due to the non-linearities and parasitic components of the circuit. An alternative method is presented in [8], which models the delay stage as a *RC* circuit. This method is also employed in [9], however, the approach suggested by the authors is based on the premise that the voltage waveform is sinusoidal, producing equations where the unique variable is the oscillation frequency. Another approach can be found in the paper [10] where an analytical approach to estimating the RO's oscillation frequency was suggested.

Therefore, this paper proposes a fast simulation-based method to estimate the main RO parameters. Since the proposed method avoids transient simulations and only uses AC ones over DC sweeps, the RO parameters can be obtained almost instantaneously, consuming less computation resources than traditional methods. The remainder of the paper is organized as follows. Section II presents the proposed characterization method from simulations, addressing the modeling of the RO implemented with two types of inverters: traditional (INV) and Schmitt trigger (ST). The Section III shows the resulting characterization of each RO, based on both INV and ST, obtained from the simulation method using Cadence Spectre in a 180 nm CMOS process. Concluding remarks are made in Section IV.

II. Characterization Method

A. Ring Oscillator Modeling

The small-signal model of the CMOS RO is shown in Fig. 1, in which each stage can be modeled by: the inverter effective transconductance (g_m), the inverter output resistance (R_o), and the stage capacitance (C_o). It should be observed that C_o also includes the input and output capacitance of the inverter.

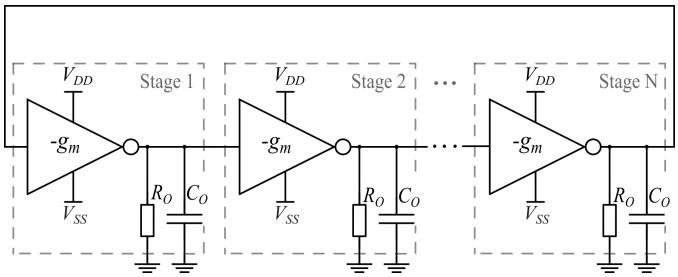


Fig. 1. Schematic circuit of the *N*-stages Ring Oscillator (RO).

Therefore, the corresponding transfer function of the RO is given by

$$G(j\omega) = \left(\frac{A}{1 + j\omega R_o C_o} \right)^N , \quad (2)$$

where A denotes the absolute gain of one stage ($A = g_m/g_o$) and N is the number of RO stages. Note that R_o can also be expressed as the inverse output conductance (g_o).

In order to estimate the minimum gain and oscillation frequency required to start the oscillation, we can apply the Barkhausen criterion. This criterion states that, in a close-loop system, the oscillation can be guaranteed if the magnitude of the feedback signal is equal to unity, and the phase shift is equal to an integer multiple of 2π [11]. Therefore, the oscillation frequency and loop gain of the RO are respectively derived as

$$\omega_{osc} = \frac{1}{R_o C_o} \tan\left(\frac{\pi}{N}\right) \quad (3)$$

$$A = \sqrt{1 + \tan^2\left(\frac{\pi}{N}\right)} \approx 1 + \frac{1}{2}\left(\frac{\pi}{N}\right)^2 . \quad (4)$$

Eq. (3) shows that the oscillation frequency depends on the values of R_o and C_o, which are determined through the simulations presented in Section III. On the other hand, Eq. (4) shows the relationship between the minimum gain necessary to start the oscillation and the number of stages N of an RO, which is slightly higher than unity.

B. Inverter Modeling

Fig. 2 shows the test-benches schematic circuits to apply the proposed characterization method, from which it is possible to extract the parameters C_{o1}, C_{in2} R_{o1} and g_{m2}.

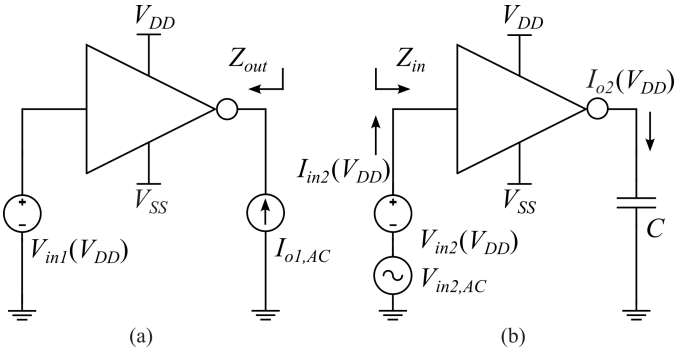


Fig. 2. Schematic circuits of the ring oscillator test bench: (a) output impedance; (b) both transconductance and input capacitance.

In the test presented in Fig. 2(a) it is injected an AC current ($I_{o1,AC}$) to the output node of the inverter, by fixing the input voltage ($V_{in1}(V_{DD})$). By this way, the output impedance Z_{out} modeled by a capacitor in parallel with a resistor, can be separated into an imaginary part and a real part as

$$C_{o1}(V_{DD}) = \mathrm{Im}\left\{ \frac{I_{o1,AC}}{V_{in1}(V_{DD})} \right\} \frac{1}{2\pi f_{AC}} \quad (5)$$

$$R_{o1}(V_{DD}) = \mathrm{Re}\left\{ \frac{I_{o1,AC}}{V_{in1}(V_{DD})} \right\}^{-1} . \quad (6)$$

A DC sweep on the supply voltage from 0 to 200 mV can be implemented for this test in order to obtain the variation of the output impedance as a function of the supply, and f_{AC} corresponds to the AC frequency of 1 kHz applied in the tests.

On the other hand, both the input impedance Z_{in} and the transconductance of the inverter can be computed by using the schematic circuit of Fig. 2(b). For this test, a huge capacitor is connected to the output of the inverter in order to measure the output current $I_{o2}(V_{DD})$, which is used to estimate the transconductance, yielding

$$g_{m2}(V_{DD}) = \mathrm{Re}\left\{ \frac{I_{o2}(V_{DD})}{V_{in2,AC}} \right\} . \quad (7)$$

Additionally, by neglecting the effect of the real part of Z_{in}, C_{in} is computed by using the input current $I_{in2(V_{DD})}$ and the input voltage $V_{in2,AC}$ as

$$C_{in2}(V_{DD}) = \mathrm{Im}\left\{ \frac{I_{in2}(V_{DD})}{V_{in2,AC}} \right\} \frac{1}{2\pi f_{AC}} . \quad (8)$$

C. Estimation of The Ring Oscillator Parameters

Since the described parameters are functions of the supply voltage V_{DD}, and in order to have a more practical design values, in this work we propose to estimate all the parameters as the effective value. The effective value is computed as the integral with respect to the supply voltage over the supply voltage range, yielding

$$\overline{C_o} = \frac{1}{V_{DD}} \int_0^{V_{DD}} [C_{o1}(V_{DD}) + C_{in2}(V_{DD})] \, \mathrm{d}V_{DD} \quad (9)$$

$$\overline{R_o} = \frac{1}{V_{DD}} \int_0^{V_{DD}} [R_{o1}(V_{DD})] \, \mathrm{d}V_{DD} \quad (10)$$

$$\overline{g_m} = \frac{1}{V_{DD}} \int_0^{V_{DD}} [g_{m2}(V_{DD})] \, \mathrm{d}V_{DD} . \quad (11)$$

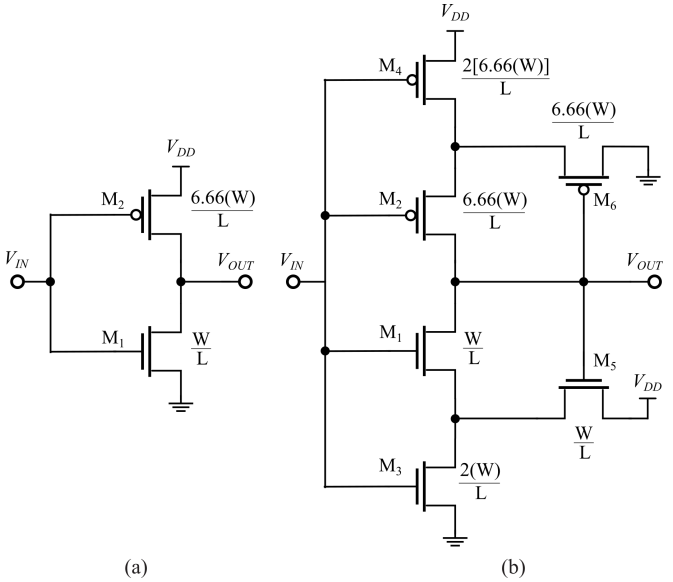


Fig. 3. Schematic circuits of characterized inverters: (a) traditional (INV); (b) Schmitt Trigger (ST).

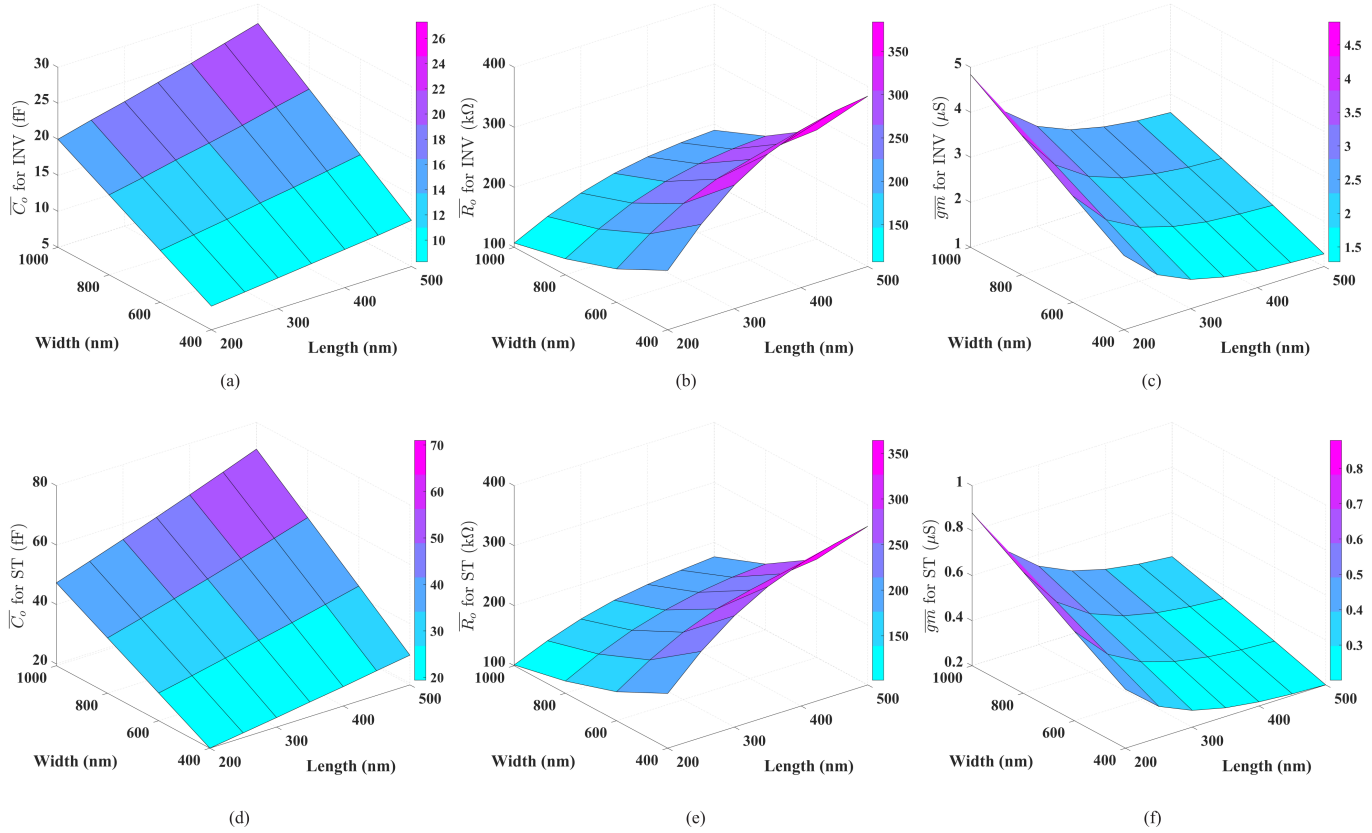


Fig. 4. Average values of output capacitance, output resistance and transconductance for inverters INV and ST, which were computed from Eqs. (9), (10) and (11), respectively.

III. Characterization Method for INV and ST Inverters in 180 nm CMOS

In order to perform the described simulation-based method, we proposed to apply the same procedure for two types of inverters, the traditional inverter (INV) and the Schmitt Trigger (ST) one, which are displayed in Fig. 3(a) and Fig. 3(b), respectively. Simulations were carried out using a 180 nm CMOS process in Cadence/Spectre.

The proposed characterization method was applied for various transistor dimensions and is described in Table I. In order to maintain the mobility compensation between PMOS and NMOS devices, the ratio of PMOS was chosen to be 6.66 times bigger than NMOS. The dimension description for each transistor in INV and ST inverters can be appreciated in details in Fig. 3.

TABLE I
Sweep Description of Transistor Dimensions

Parameter	Initial value	Final value	Step
W	400 nm	1 μm	200 nm
L	200 nm	500 nm	50 nm

Fig. 4 shows the obtained results for the average values $\overline{R_o}$, $\overline{C_o}$ and $\overline{g_m}$, computed from Eqs. (9), (11) and (10), respectively. In all simulations, a voltage range from 0 to 200 mV was used, and 1 kHz frequency was used for all AC quantities presented in Fig. 2. In addition to the detailed characterization for each RO parameter presented in Fig. 4, the operation frequency of the RO can be approximated by (see Eq. (3))

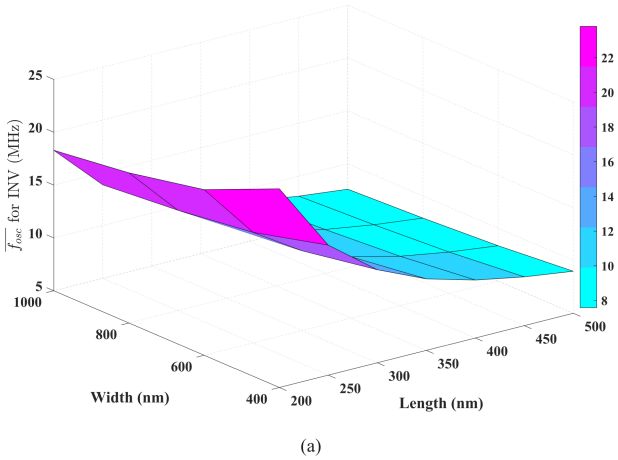
$$\overline{f_{osc}} = \frac{1}{2\pi} \frac{1}{(\overline{R_o} \cdot \overline{C_o})} \tan\left(\frac{\pi}{N}\right) . \tag{12}$$

In order to compare the RO characterization method regarding transient simulations of the RO, a 13-stage RO was employed. Fig. 5 shows the results for the oscillation frequency of the inverter INV. As can be appreciated, the frequency extracted from transient simulations in Fig. 5(b) has close behavior to the one obtained by our method in Fig. 5(a), keeping a relative error lower than 20%, and avoiding the extensive transient simulations.

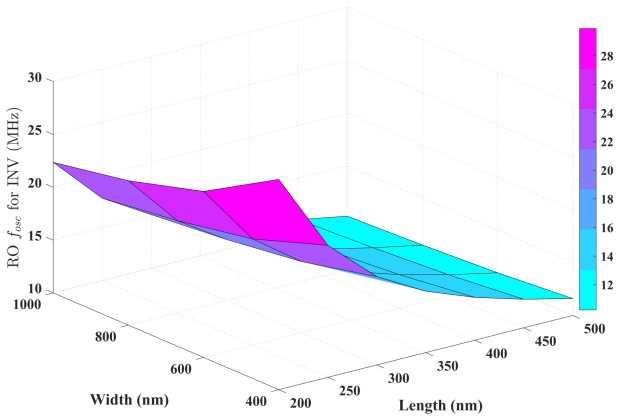
On the other hand, Fig. 6 shows results for the oscillation frequency of the ST inverter. Similar to the INV case, results from our method produce results in close agreement with the transient simulation ones.

IV. Conclusions

The simulation-based method presented in this paper provides a quickly parameter estimation for CMOS ring oscillators (ROs). The main RO parameters of each unity stage,

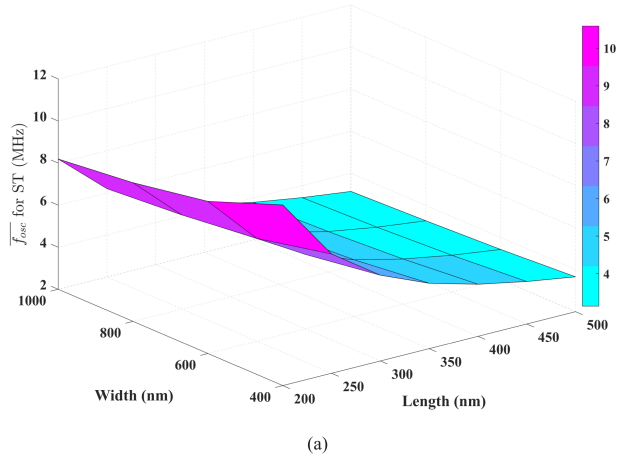


(a)

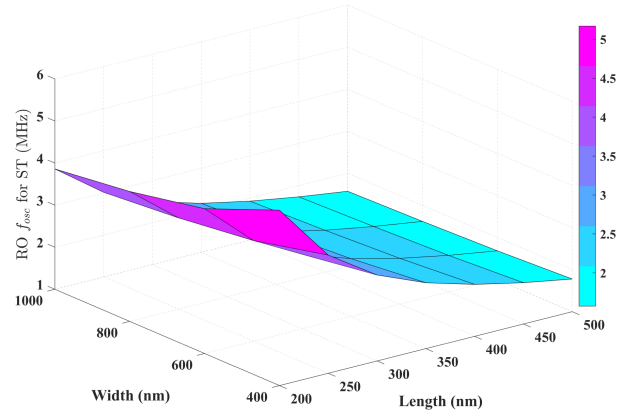


(b)

Fig. 5. Oscillation frequencies for inverter INV: (a) estimated from the proposed method (see Eq. (12)); (b) extracted from a transient simulation of the RO circuit with 13-stage.



(a)



(b)

Fig. 6. Oscillation frequencies for inverter ST: (a) estimated from the proposed method (see Eq. (12)); (b) extracted from a transient simulation of the RO circuit with 13-stage.

such as the output capacitance, transconductance, and output resistance, were determined by performing a transistor dimension sweep using a low-voltage range from 0 to 200 mV. Hence, an additional estimation of RO oscillation frequencies was computed, allowing to assess the complete RO behavior at various dimensions. As appreciated from the comparison of analytical with simulated results, the parameters did not produce exact estimation, but kept the same behavior regarding transistor dimension, which can be useful to obtain an initial and fast RO design at the employed CMOS process.

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